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(54) METHODS AND CIRCUITS FOR SENSING

VOLTAGE ACROSS THE ISOLATION BARRIER

3/3353 (2013.01); *H02M* 3/33515 (2013.01);

(2013.01)

(58) Field of Classification Search

See application file for complete search history.

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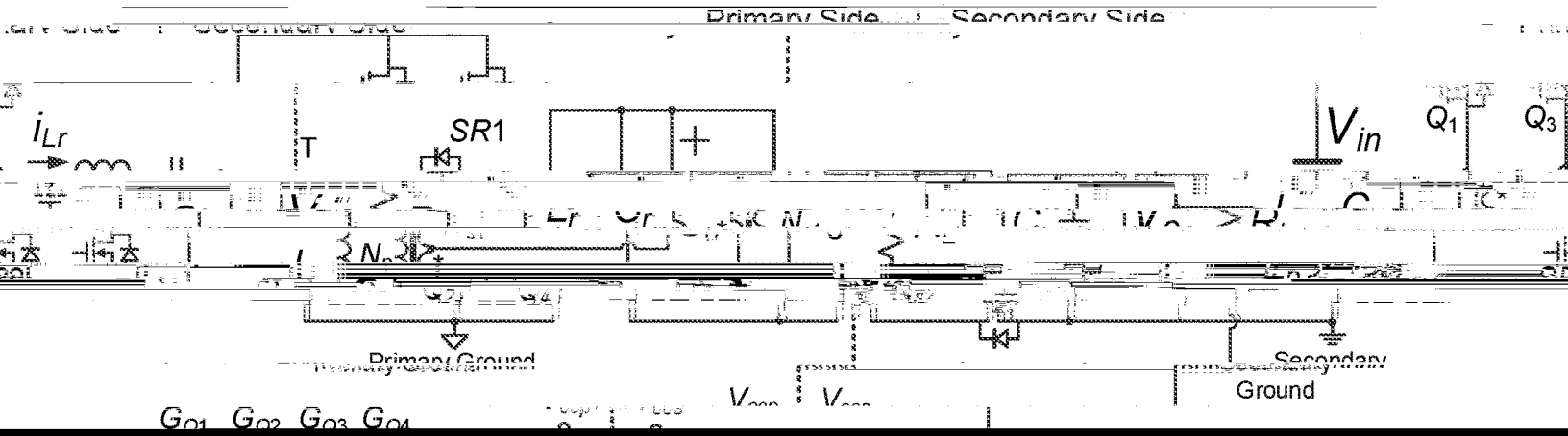
363/17

U.S. PATENT DOCUMENTS

363/21.02


Primary Side
Secondary Side
i_{Lr}
T
SR1
V_{in}
Q_1
Q_3
Primary Ground
Secondary Ground
G_{Q1} G_{Q2} G_{Q3} G_{Q4}

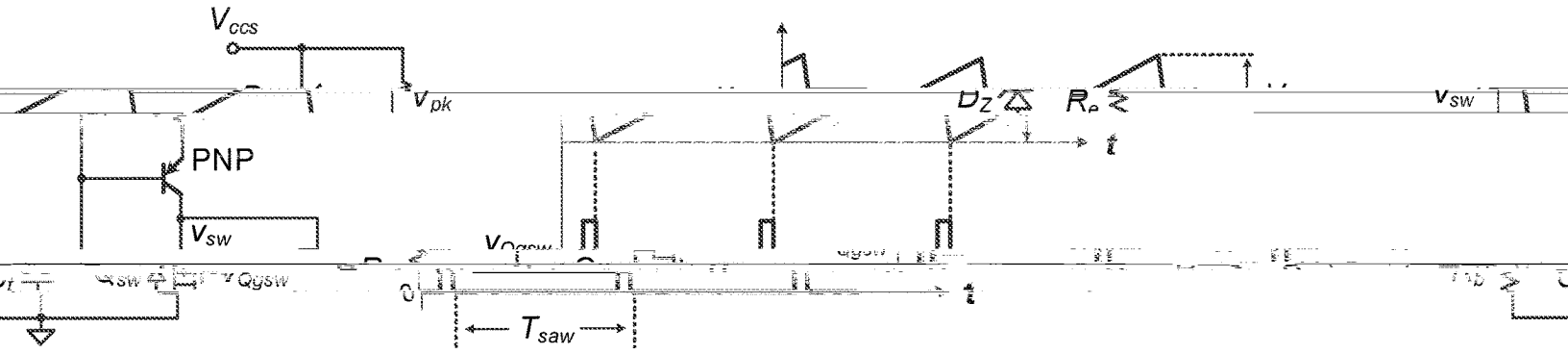
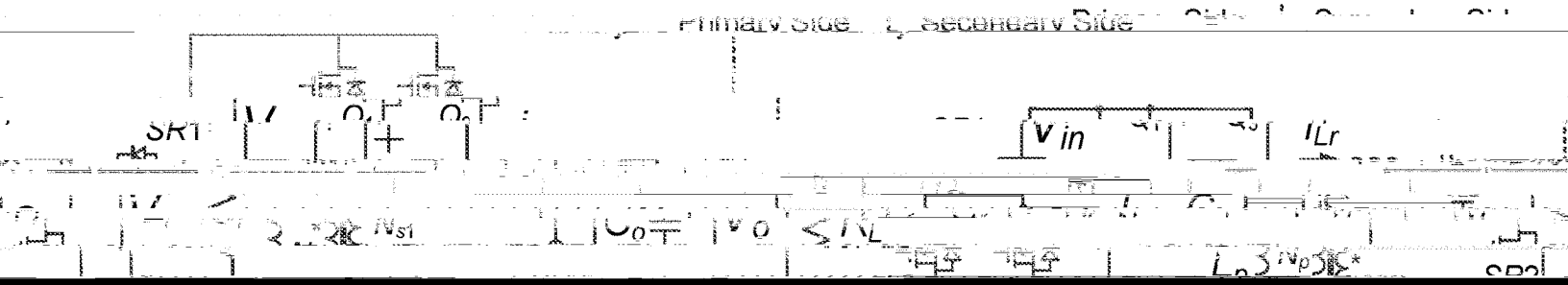
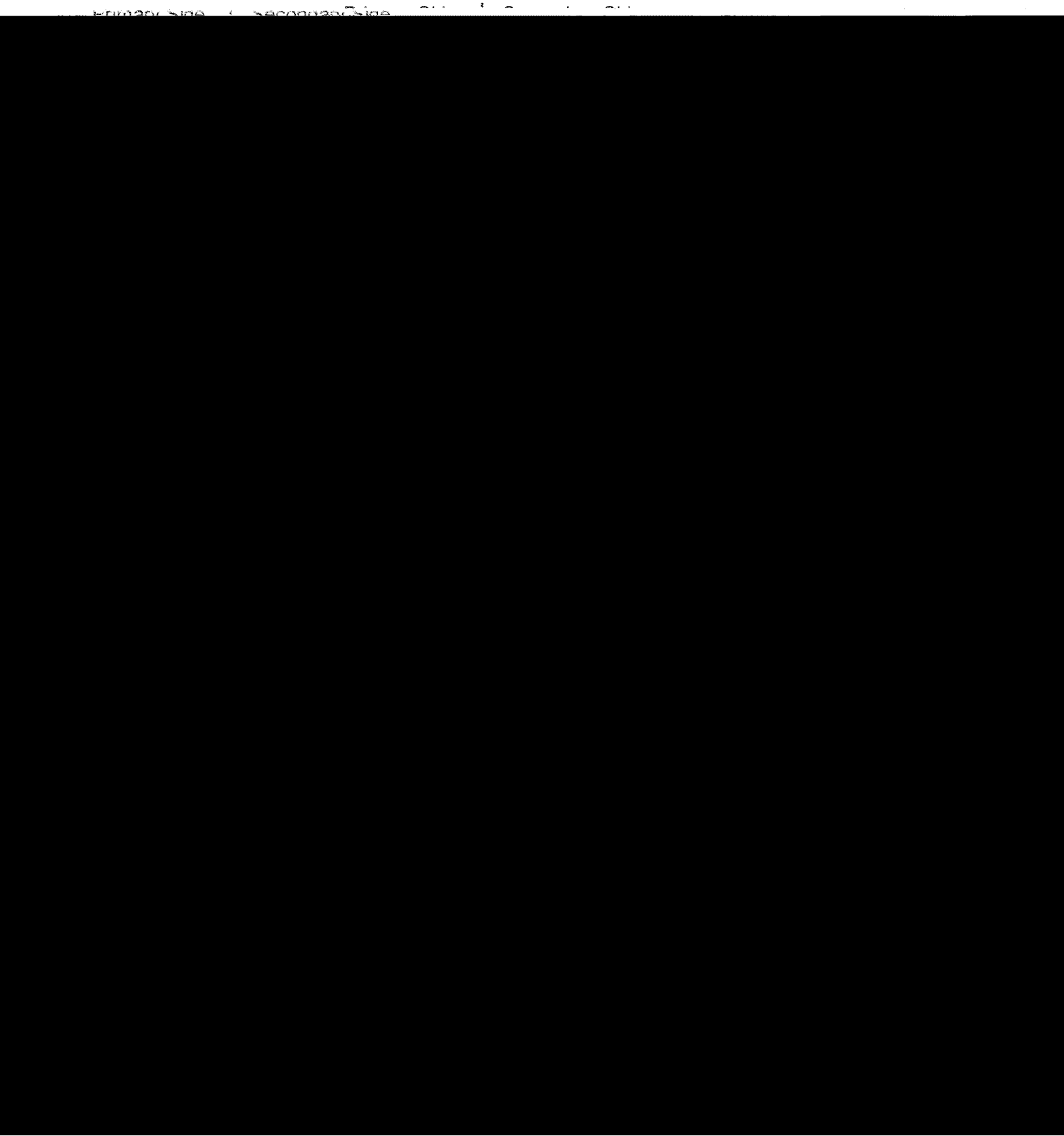
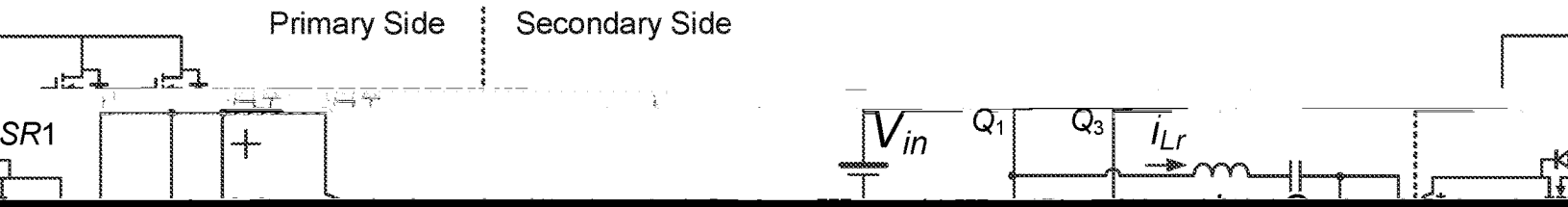


Fig. 4 (Prior Art)


Primary Side
Secondary Side
SR1
SR2
Vin
iLr


Primary Sine
Secondary Sine


Primary Side
Secondary Side
SR1
V_{in}
Q_1
Q_3
i_{Lr}

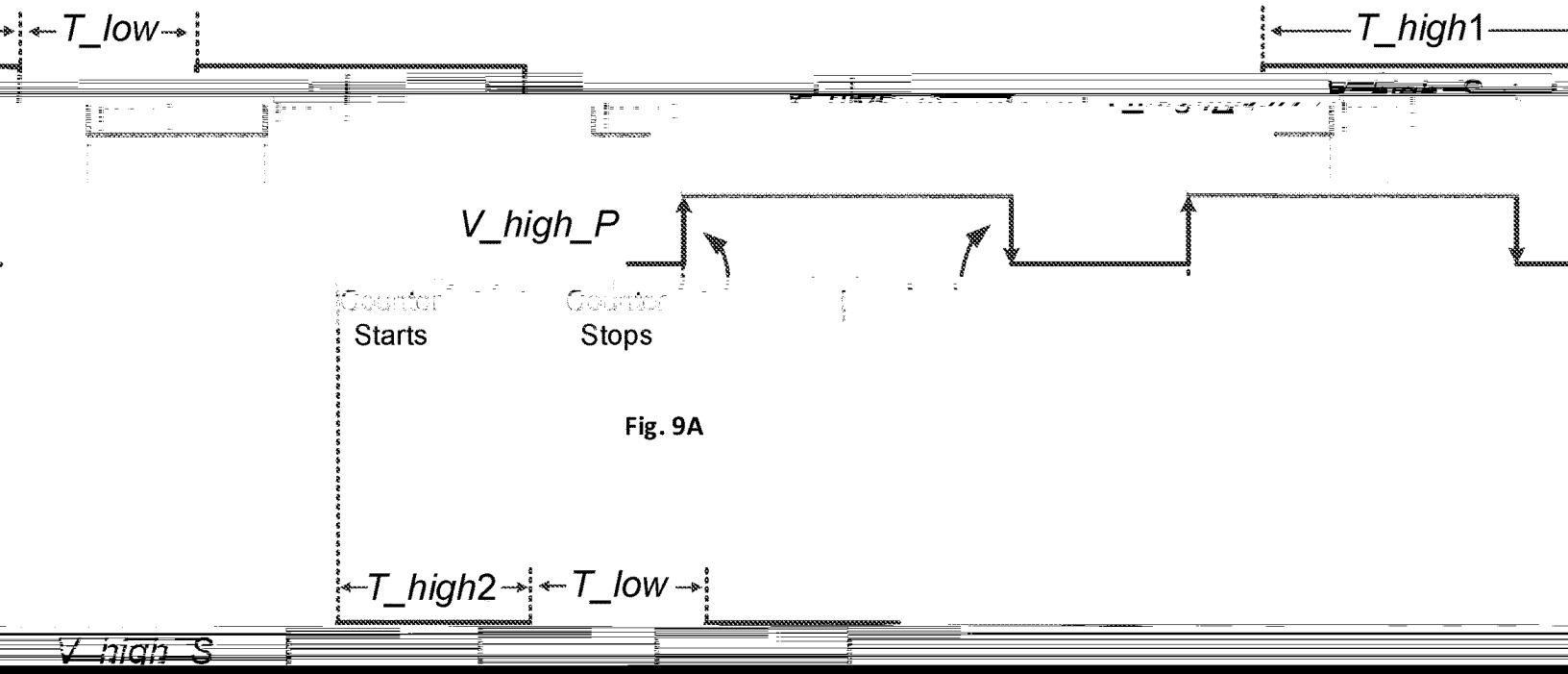
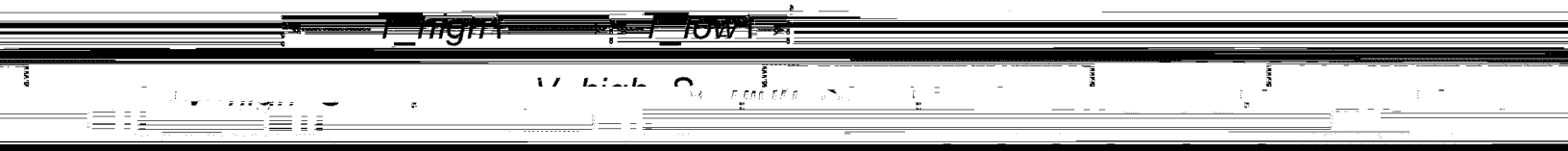

T_low
T_high1
V_high_P
Counter Starts
Counter Stops
T_high2
T_low
V_high_S

Fig. 9A


T_high1
T_low1

iment the first sensing circuit comprises a

ment the control circuit includes a feedback

barrier to the primary side of the isolated power converter;

wherein a steady state output voltage is determined using the reference voltage; wherein the first microcontroller calculates a steady state value of the steady state output voltage using the steady state gain to calibrate an actual gain of the first

accurate sensing of the output voltage of isolated power

primary side power switching devices of the isolated power

METHODS AND CIRCUITS FOR SENSING

In one embod

In one embodi

circuit comprising: a second sensing circuit that senses the

Application No. 63/188,732, filed on May 14, 2021, the

isolator that transfers the error voltage across the isolati

contents of which are incorporated herein by refer

their entirety.

this invention relates to

specifically, the invention

sensing circuit to the determine an actual se

output voltage; wherein the first microcontroll

the converter isolation barrier to achieve accurate output

secondary side output voltage from the control signal and converter to regulate the secondary side output voltage at a selected value.

In one embodiment the control signal is produced using a

primary side power switching devices of the isolated power

using the value of the sec

control primary side power

herein.

or a digital isolator OP2. The optocoupler or digital isolator improved by automatically calibrating its steady state oper-

gic signal from the secondary side to primary ating point with the output voltage feedback loop using an transfers the

For example if at steady state the output voltage is Vo=30V, Vo sensing

Therefore, if the measured Vop is 2.5V, the actual output

). Similarly, if measured Vop

3.5V, the actual output voltage Vo can be predicted as 35V

elay is not desired, or even not allowed.

be substantially avoided by the embodi-

voltage Vo is converted into a PWM signal V_{PWMS} using a comparator and sawtooth wave Vsw. T_high is the logic high time interval of that PWM signal and is proportional to

power supply turns on, the temperature inside the power supply

ter. The peak value of the sawtooth

signal is Vpk_25. If the power supply temperature rises to

100° C., the peak value of the sawtooth signal may change

to Gain_100. With the calibration loop including an error amplifier and analog optocoupler, the actual gain of the PWM Vo sensing circuit

(9). The falling edge

If the LLC converter used is a single stage AC to DC

discharged to zero. The

peak value of C1, Vpk1 (=Vop),

taking the average of the sampled Vop voltage over the

actual gain of the PWM_Vo sensing circuit with PFC

CE2=100 nF, the delay time is estimated as around 200 us.

). Similarly, if measured Vop will take Vop about 200 us to change from 3V to 3.3V. This

3.5V, the actual output voltage Vo can be predicted as 35V

delay should be considered in the design. In some applications, this delay

elay is not desired, or even not allowed.

(=3.5V/0.1). With the accurately measured output voltage, the primary side MCU2 can achieve accurate output over

primary side as 25V (=2.5V/0.1

tions, this d

Such delay may

actual output voltage to achieve better closed loop performance.

In some embodiments the calibration process may be

V_{PWMP} is used to control the on and off operation of the

off and the capacitor C1 is charged by constant current

rises linearly. At the end of T_high, the voltage at C1 is

V_{PWMP} is at logic high level,

$$T\_high=T\_high*(Vz-0.7)/Re/C1 \quad (9)$$

$$Vop-Vpk1=IC1*$$

$$Vpk*(Vz-0.7)/Re/C1 \quad (10)$$

[illegible]

[illegible] of the fast PWM Vo sensing circuit may be updated con[illegible]

[illegible] Courtesy,

[illegible] 9A, is assumed that when Vo is at steady state value, s[illegible]

[illegible] as 30V, MCU1 will produce a logic high time of 10

[illegible] Accurate PWM Vo Sensing

[illegible] ferred to the

[illegible] Another embodiment, shown in FIG. 7, provides an [illegible] T_high1=10 us. This signal (V_high_S) is trans[illegible]

[illegible] accurate PWM Vo sensing circuit that achieves accuracy of [illegible]

[illegible] 3% or better. In this circuit, another digital controller MCU2 [illegible] V_high_P. The T[illegible]

high value is same for V_high_S and [illegible] is used at the secondary side. The output voltage Vo is sensed [illegible]

proportional to the actual value of Vo. Using the calibration

comparator that produces the PWM signal.

sensing

with respect to the embodiment of FIG. **8** may also be used

pulse width of the Vo PWM signal and therefore

to detect the actual output voltage Vo. The details would be

high) of the PWM signal and uses the

contents of all cited documents are incorporated

n the second
voltage com-
or voltage

wherein the first microcontroller samples a voltage across the capacitor at a sampling time set by a period of the

rising time of the PWM signal.

to calibrate the Vo PWM signal to remove the possible error

introduced because of the inherent delay time of the digital

isolator or optocoupler and to improve the accuracy of the

that senses the secondary side output voltage comprises a

outputs the PWM signal to the first microcontroller;

wherein the first microcontroller measures a logic high

apparent to one skilled in the art based on the embodiments

described above.

EQUIVALENTS

While the invention has been described with respect to illustrative embodiments thereof, it will be understood that various changes may be made to the embodiments without departing from the scope of the invention. Accordingly, the

the invention is not to be limited thereby.

selected value.

7. The control circuit of claim **1**, wherei
circuit that senses the secondary side output
prises an error amplifier that produces the err

side circuit comprises a sampling circuit including a capaci-

power converter;

output voltage;