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Primary Side

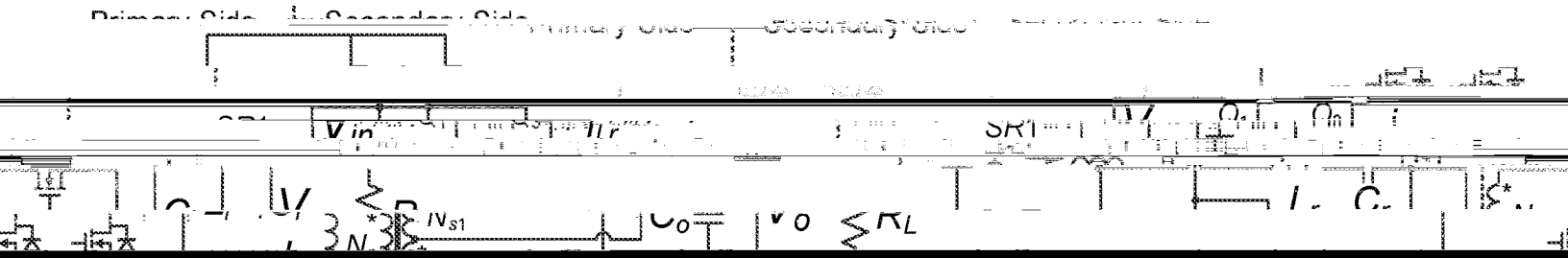
Secondary Side





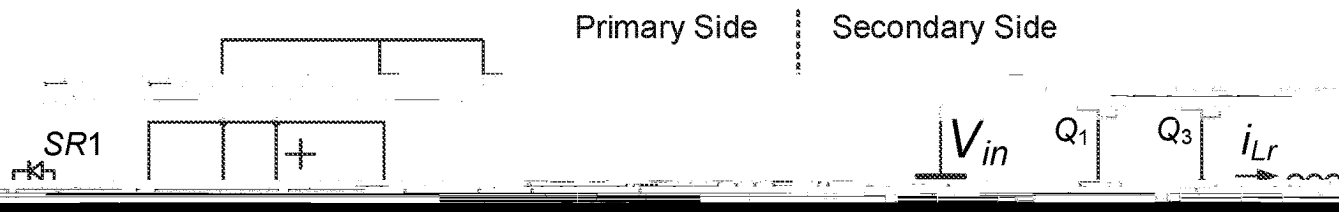


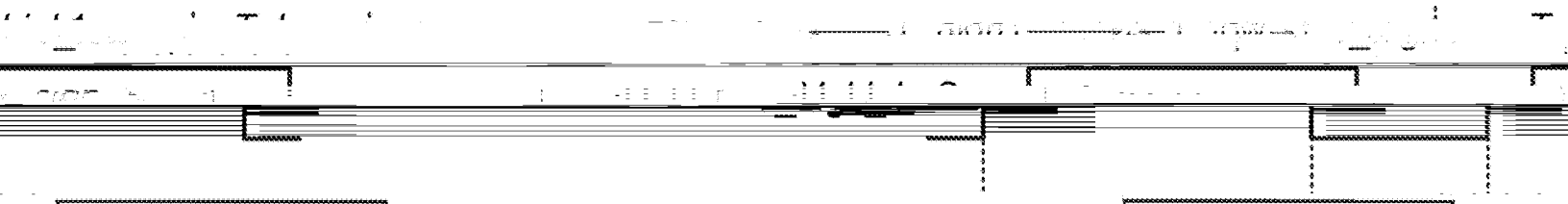




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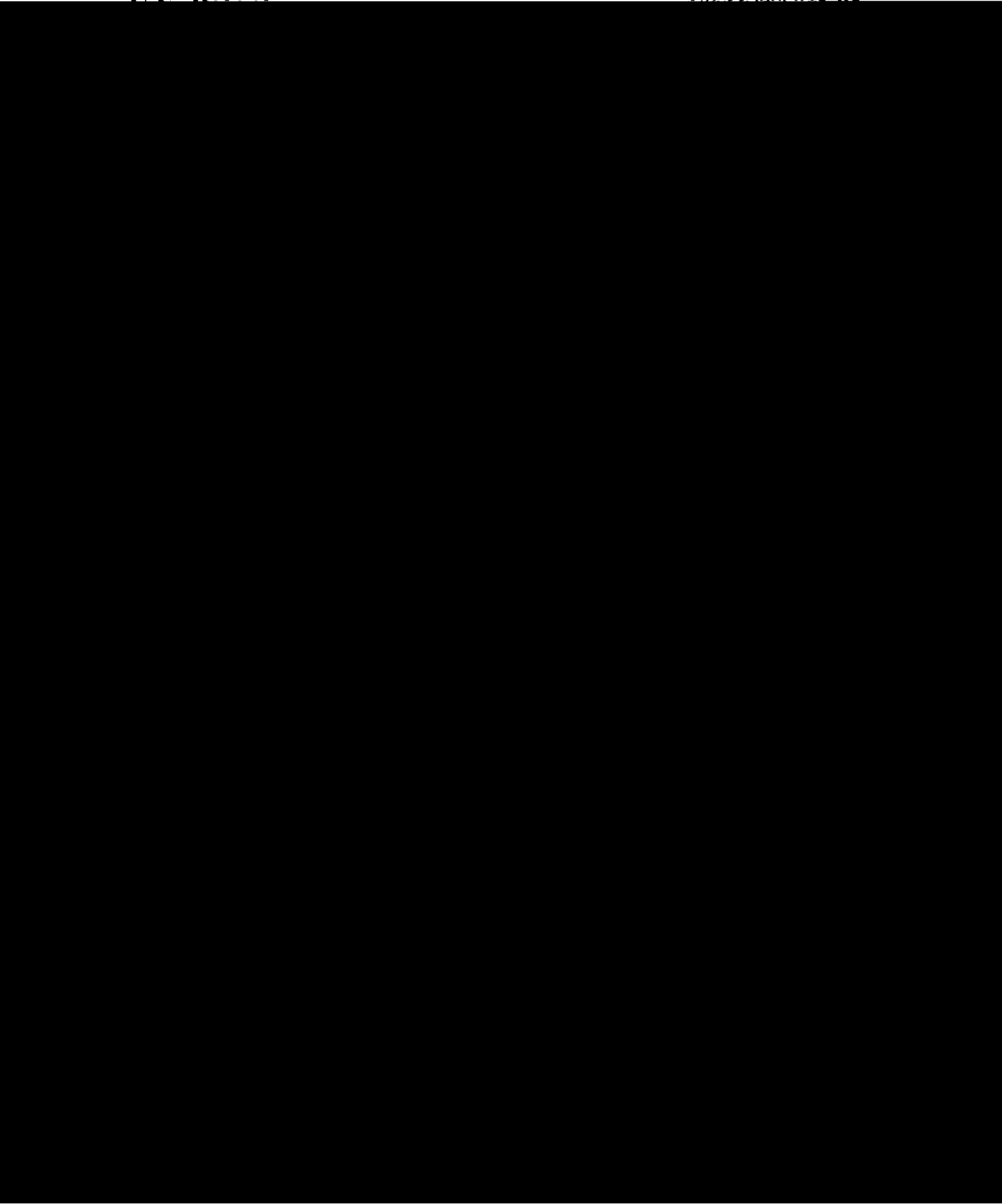
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isolator at the primary side to produce a control signal; and primary side power switching devices of the isolated power

output voltage at using a first microcontroller to determine the value of the converter to regulate the secondary side

using the value of the secondary side output voltage to Another aspect of the invention relates to an isolated

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FIG. 11 is a schematic diagram of a  $V_o$  sensing circuit according to one embodiment. The circuit provides a signal that is directly proportional to the value of the output voltage from one side of the isolation barrier (secondary side) to the other side of isolation barrier (primary side).





For example, if it suddenly starts, the output voltage is  $V_o = 20V$ .  $V_o$  remains. If  $V_o$  has a very fast change, the  
 and the voltage measured by ADC12 of MCU2 is changing instantly. For example, if the converter's frequency is  
 $V_o = 20V$  and the measured  $V_{op}$  is  $20V/0.1 = 200V$ . For  $100kHz$ ,  $DE1 = 200V$ ,  $CE1 = 150pF$ ,  $DE2 = 150pF$   
 voltage,  $V_o$ , can be predicted accurately by MCU2 at the  $3$ . This means that if  $V_o$  changes quickly from  $20V$  to  $30V$ , it  
 primary side of  $25V$  ( $= 25V/0.1$ ). Similarly, if measured  $V_{op}$  will take  $V_{op}$  about  $200ns$  to change from  $20V$  to  $30V$ . This

the primary side MCU2 can achieve accurate output over Such delay may be substantially avoided by the embodi-

such as the feedback and control under load regulation. The delay of the feedback loop can be reduced by the embodi-

side requires additional calculations based on the with very small delay. At the secondary side, the output

accurate PWM Vo sensing circuit that achieves accuracy of

primary side, by the optocoupler, or digital isolator, as

The duty cycle of the second PWM signal (Vo PWM) is ... power converter:

to calibrate the Vo PWM signal to remove the possible error ... calculates a steady state gain in response to the steady state ... introduced because of the inductor or capacitor of the power converter.

output voltage, and uses the steady state gain to calculate the steady state output voltage of the power converter.

use of the inherent delay time of the digital output voltage, and uses the steady state gain to calculate the steady state output voltage of the power converter.

simultaneously and to measure the accuracy of the measured output voltage of the power converter.

PWM Vo sensing. determine an actual secondary side output voltage; wherein the first primary side circuit controls the primary side power switching devices of the isolated power converter.

Similarly, the T<sub>high</sub> time detection method as described in FIG. 10, with respect to the embodiment of FIG. 9 may also be used.

claim 4, wherein the second apparent to one skilled in the art based on the embodiments described above.

The circuit comprises an error amplifier that produces the error voltage.

The control circuit of claim 1, wherein the first primary side circuit produces the error voltage.

uses a duration of the T<sub>high</sub> interval of the PWM signal to determine a magnitude that is proportional to the secondary side output voltage.

5. The control circuit of claim 1, wherein the first primary side circuit produces the error voltage.

6. The control circuit of claim 1, wherein the first primary side circuit produces the error voltage.

EQUIVALENTS

illustrative embodiments thereof, it will be understood that various changes may be made to the embodiments without departing from the scope of the invention. Accordingly, the described embodiments are to be considered exemplary and the invention is not to be limited thereby.

25 comprising:

power converter using a first secondary side circuit that produces a pulse width modulation (PWM) signal that is proportional to a value of the secondary side output voltage;

and uses the measured magnitude of the generated voltage to determine the value of the secondary side output voltage.

7. A method for controlling a n isolated power converter, comprising:

sensing a secondary side output voltage of the isolated power converter;

50 senses a secondary side output voltage; and

uses the sensed secondary side output voltage to determine a magnitude that is proportional to the secondary side output voltage.

logic high time (T<sub>high</sub>) interval that is proportional to a value of the secondary side output voltage.

35 using a first primary side circuit to receive the PWM signal.

power converter using a first secondary side circuit that produces a pulse width modulation (PWM) signal that is proportional to a value of the secondary side output voltage;

and uses the measured magnitude of the generated voltage to determine the value of the secondary side output voltage.

7. A method for controlling a n isolated power converter, comprising:

sensing a secondary side output voltage of the isolated power converter;

plung circuit including a capacitor that is charged and discharged according to the T<sub>high</sub> interval of the PWM signal; and a switch that shapes the PWM signal received from the first isolator by reducing a falling time and rising time of the PWM signal;

plung circuit including a capacitor that is charged and discharged according to the T<sub>high</sub> interval of the PWM signal; and a switch that shapes the PWM signal received from the first isolator by reducing a falling time and rising time of the PWM signal;

45 across the capacitor is used to determine a gain of the power converter.

across the capacitor at a sampling time set by a period of the PWM signal; and

50 wherein the sampled voltage across the capacitor is used by the processor to determine a gain of the sampling circuit and to control primary side power switching devices of the isolated power converter to regulate the secondary side output voltage.

8. The method of claim 7, wherein the first secondary side circuit comprises a comparator that produces the PWM signal.

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wherein the first primary side circuit determines a steady-state output voltage proportional to a value of the secondary side output voltage.

having a logic high time ( $T_{high}$ ) interval that is state output voltage using the reference voltage

and calculates a steady-state gain in terms of the steady-state output voltage and near the steady-state gain of the first secondary side circuit.

calculates a steady-state gain in terms of the steady-state output voltage and near the steady-state gain of the first secondary side circuit.

wherein the first primary side circuit controls the primary side power switching elements of the selected power converter to regulate the secondary side output voltage at the selected value.

wherein the first primary side circuit includes a first primary side circuit that receives the PWM signal from the first primary side circuit controller wherein the first primary side circuit controller includes a coupling circuit including a capacitor that

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