Experimental Demonstration of a Novel 5/10-Gb/s Burst-Mode Clock and Data Recovery Circuit for Gigabit PONs

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Abstract: A novel 5/10-Gb/s burst-mode receiver featuring instantaneous (0-bit) phase acquisition for any phase step (±2π) between packets in GPON is demonstrated. Our design is based on an oversampling local oscillator and a phase picking algorithm.

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1. Introduction

Gigabit-capable passive optical networks (GPONs) are an emerging multi-access network technology that provide a low-cost method of deploying fiber-to-the-home. Fig 1(a) shows an example of a GPON with our work in context. In the upstream direction, the network is point-to-multipoint: using time-division multiple access (TDMA), multiple optical network units (ONUs) transmit bursty data to the optical line terminal (OLT). Due to optical path differences, packets can vary in phase and amplitude. To deal with these variations, the OLT requires a burst-mode plcuocGTlef Tw 15.6y5(a)ypks3afe0
ith phase acquisition by a clock phase aligner (CPA). This

hase acquisition time which must be as short as possible. In
use of an oversampling CDR operated at twice the bit rate
nstrate a 5 Gb/s BMRx that achieves instantaneous (0-bit)
een consecutive packets, with packet loss ratio (PLR) < 10 -6
and bit-error rate (BER) < 10^{-10}. In addition, we achieve this in a much more cost-effective manner by employing a simple local oscillator (LO), and thus eliminating the need of complex and expensive CDR circuits based on phase-locked loops (PLLs).

2. Burst-mode receiver configuration

A block diagram of the BMRx is shown in Fig 1(b). An LO or a CDR can be used to either generate a clock signal, or recover the clock from the incoming bursty data, respectively. The CDR/LO is followed by a 1:16 deserializer from Maxim-IC (MAX3950). The lower rate parallel data is then brought onto a Virtex IV field programmable gate array (FPGA) from Xilinx for further processing. On the board, it is first necessary to further parallelize the data and clock to a lower frequency that will ensure proper synchronization and better stability of these signals before they can be sent to the CPA for automatic phase acquisition. Thus, an integrated double-data rate (DDR) 1:8 deserializer is implemented on the FPGA. Automatic detection of the payload is implemented on the

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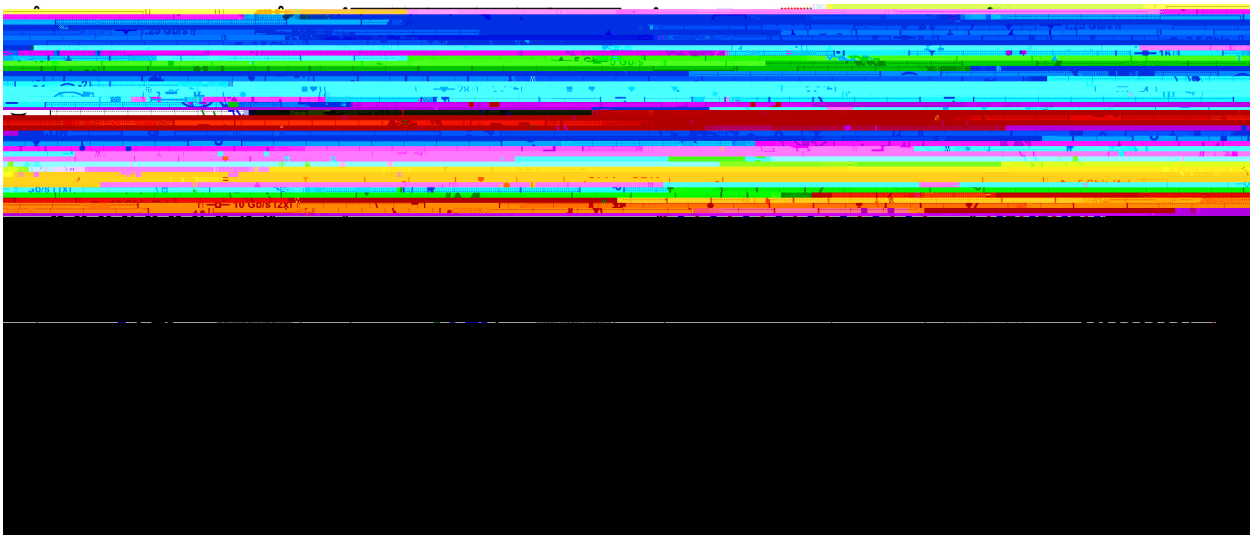

Fig 2. (a) PLR and BER vs. signal power. (b-d) PLR vs. phase step. (e) Burst-mode penalty. (f) Preamble length penalty. (g) PLR vs. CID immunity. (h) Measured input and output waveforms.

acquisition time, as demonstrated in this work, more bits are left for amplitude recovery, thus reducing the burst-mode sensitivity penalty. Alternatively, with the reduced number of bits, more bits can be used for the payload, thereby increasing the information rate.

To determine the burst-mode penalty of the receiver, we plot the PLR as a function of the received signal power in Fig 2(e). The PLR performance of the CDR sampling continuous data at the bit rate with no phase difference is compared to the PLR performance of the BMRx sampling bursty data with a worst-case phase difference, $\Delta\varphi = \pi/2$ rads. Both measurements are made for a 0-bit preamble. We observe a power penalty of less than 1 dB due to 2× oversampling and the phase picking algorithm. If there does exist a worst-case phase difference between the