A 10-Gb/s Space Sampling Burst-Mode Clock and Data Recovery Circuit for Passive Optical Networks

Bhavin J. Shastri and David V. Plant
Photonic Systems Group, Dept. of Electrical and Computer Eng., McGill University, Montreal, QC H3A 2A7, Canada
shastri@ieee.org

***Abstract*—We demonstrate a novel 10-Gb/s burst-mode CDR circuit for PONs featuring instantaneous (0-bit) phase acquisition with BER < 10 ^{11}. Our design is based on hybrid topology: feedback CDR and feed-forward clock phase aligner utilizing space-sampled clocks.**

I. Introduction

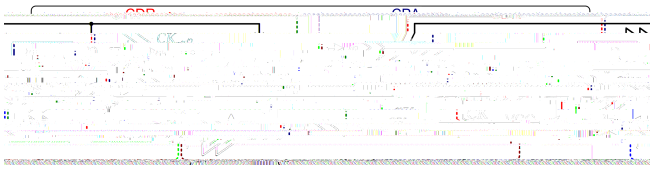
Passive optical networks (PONs) are recognized as an economic solution to alleviate the bandwidth bottleneck in access networks by deploying fiber-to-the-home. The challenge in the design of a chip set for PONs arises from the upstream data path as the network is point-to-multipoint. Using time division multiple access, multiple optical network units (ONUs) transmit data to the optical line terminal (OLT) in the central office. Due to optical path differences, the data received at the OLT is inherently bursty with asynchronous phase steps $j \quad 'j \quad 2$ rad with a bit-error rate (BER) < 10

^{11}.

II. Novel BM-CDR Architecture

A block diagram of the proposed BM-CDR is shown in Fig. 1. The BM-CDR is composed of a phase-tracking CDR and a clock phase aligner (CPA). The CDR senses data D_{in}, and generates a synchronized clock CK, with a voltage-controlled oscillator (VCO) in a phase-locked (feedback) loop (PLL). The phase and frequency of CK is compared to D_{in} in the phase/frequency detector (PFD), generating an error signal that is passed through the charge pump (CP) and the low-pass filter (LPF) to set the voltage required by the VCO to oscillate at the frequency of interest.

Burst-mode functionality is obtained with the CPA which utilizes multi-phase clocks and a phase picking algorithm



$_{\text{in}}$, with consecutive clock CK_o edges, at multiple points in the vicinity of expected transitions [see Fig. 2(a)], resulting in three data samples: previous bit A, current bit B, and a sample of the current bit at the zero crossing T. Depending on the phase difference between the consecutive packets, the PD aided by these samples, $X \quad T \quad B$ and $Y \quad A \quad T$, can determine the location of the clock edge with respect to the data edge as follows: (a) if A and B

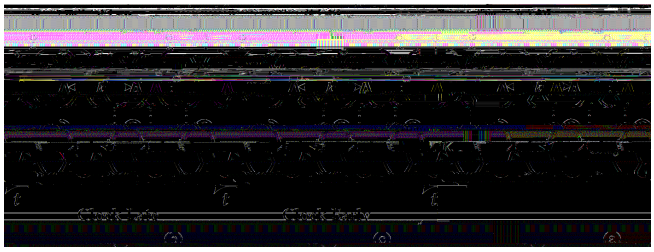


Fig. 2. (a) Three-point sampling scheme; (b) and (c) early-late waveforms.

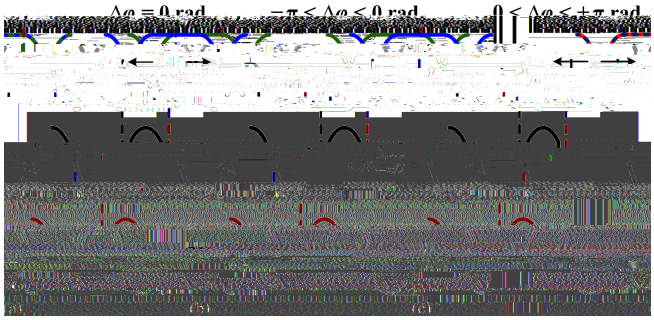


Fig. 3. CPA phase picking algorithm.

That is, regardless of any phase step, there will be at least one clock, either $CK_{\quad =2}$ or $CK_{+\ =2}$, that will yield an accurate sample. The -picker then selects the most accurate clock CK_{out}, from these two possibilities for driving the D-FF to retime the data; that is, sample the noisy data, yielding an output D_{out} with less jitter.

III. E