A 20-GSample/s (10 GHz × 2 clocks) Burst-Mode CDR Based on Injection-Locking and Space Sampling for Access Networks

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Abstract: We demonstrate a novel 20-GSample/s burst-mode CDR circuit featuring instantaneous (0-bit) phase acquisition with BER<10^{-10} for any phase step ($\pm 2\pi$ rad) between successive bursts. Our design incorporates injection-locking and space sampling for clock phase recovery/alignment.

1. Introduction

As the explosive growth in Internet traffic continues, the need for highly-specialized low-cost integrated circuits is undeniable, with clock and data recovery (CDR) being a critical function in back plane routing and chip-to-chip interconnects. Furthermore, the traffic received on these multiaccess links—passive optical networks [1] and packet-switched networks [2]—is inherently bursty with asynchronous phase steps $|\Delta\ |$ 2π rad, that exist between the consecutive k^{th} and $(k+1)^{th}$ packets. This inevitably causes conventional CDR circuits to lose pattern synchronization leading to packet loss. Preamble bits can be inserted at the beginning of each packet to allow the CDR feedback loop enough time to settle down and thus acquire lock. However, the use of a preamble reduces the effective throughput and increases delay. Consequently, to deal with bursty data, these networks require a burst-mode CDR circuit (BM-CDR).

Recently, BM-CDRs that achieve instantaneous phase acquisition have been demonstrated [1][2]. These BM-CDRs

Fig. 1. Block diagram of the proposed BM-CDR.