Frontiers in Optics + Laser Science 2023 (FiO/LS) © Optica Publishing Group 2023

Fully Integrated Photonic Tensor Core Accelerator for Neural Network Applications

N. Peserico[1,2], X. Ma[1], B. Movahhed Nouri[1], H. Dalir[2], B. J. Shastri[3], V. J. Sorger[1,2]

1. Department of Electronics and Computer Engineering, George Washington University, 800 22nd St, 20052, Washington, DC, USA
2. Department of Electrical and Computer Engineering, University of Florida, Gainesville, Florida 32611, USA
3. Department of Electronics and Computer Science, Queens University, Kingston, Canada

volker.sorger@ufl.edu

***Abstract*— Machine Learning applications have exploded in recent times. Here, we present the first fully-integrated Photonic Tensor Core accelerator, capable of computing Neural Networks by integrating all the optical components, from laser to photodetectors.**

Keywords*— *Silicon Photonics, Packaging, Neural Networks, Laser, Heterogeneous Integration

I. INTRODUCTION

The new industrial revolution is being driven by applications of artificial intelligence, namely Machine Learning (ML) applications based on Neural Networks, which have recently begun to reach their full potential [1]. How far ML can advance for the general audience has been demonstrated by applications for text generation and complicated image synthesis. However, since those networks are now working with billions of parameters for every single inference, training could take weeks for a data center to run, with the related high energy consumption of up to millions of dollars [2]. The need for a quicker and more effective method to compute matrix multiplication for neural networks is critical given the growth of ML applications. 5], two important comp

Here, we present our Fully Integrated Ph
Silicon Photonics technology for high-speed
carrier without any need for fiber coupling, f

ESIGN AND RESULT

A. *Photonic Tensor Core Design*

The proposed PTC is formed by a main Sil
ors, which multiply the signals by dividing the optical power between the two output

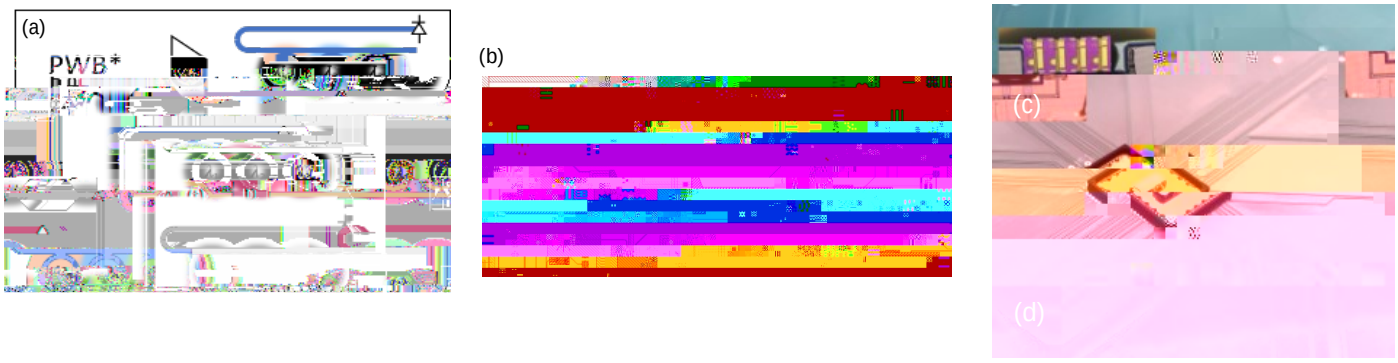

Figure 1: Scheme and photo of the realized Photonic Tensor Core. (a) Scheme of the PTC, with integrated laser sources, input vector encoding modulators, microring modulators weight matrix, and balanced photodetectors. (b) GDS design of the PTC. (c)

branches. The output power is collected by two SiGe photodetectors. The silicon photonic chip has been realized by AIM Photonics using one of its Silicon Photonic active MPW shuttle runs. A 4-fold InP DFB laser bar is used to create the lasers, and it is embedded inside a silicon photonic chip with a deeply etched cavity (Fig. 1c). The photodetectors, as well as the vector and matrix encoding components, have been chosen to achieve the highest speeds and Signal-to-Noise Ratios possible (Fig. 1b).

The entire heterogeneous integrated chip has been packed inside a QFN carrier, creating the first "photonic black box" in which all of the optics are contained within the carrier and only electrical I/O is provided (Fig. 1d). Without the use of fiber arrays or external laser sources, this sort of packaging enables the integration of one or more photonic chips into intricate electrical circuits.

B. Initial Results

As a first step to test the chip, we used a grating coupler placed after the Mach-Zehnder Modulator (MZM), which encodes the input vector, to evaluate the laser's reaction following integration. Around 1 dB is thought to be the PWB's predicted Insertion Loss. However, issues with the first batch of Silicon Photonic chips caused a number of the tapers that have to couple the PWB with the silicon waveguide, to be damaged, leading to a greater than anticipated IL (>20 dB), on top of the losses from the circuit's components. However, as the lasers exhibit good linewidth and are in good accord with the findings of the wafer-level datasheet, we examine the integrated laser spectrum at various current levels (Fig. 2nishem osir61.7 (a)4.3 (t)18.9 (e)16.3 od to be 2ci(o)19 (o)12.d (h)1 (c)]TJ-0.006 Tc16