Fully Integrated Silicon Photonic Tensor Core for Next-Generation Applications

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Abstract: Here we present our architecture for Silicon Photonic Tensor Core, capable of responding to the needs of Neural Networks, Augmented and Virtual Reality applications. We present a novel version fully integrated, from lasers to photodetectors.

1. Introduction

With the explosion of data-based applications, where fast elaboration of the incoming data streams from different sources is required, the request for highly specialized hardware accelerators has increas

integrates all the needed components, from the lasers (using Photonic Wire Bonding) to the high-speed photodetectors.

2. Results

The PIC exploits a WDM scheme, where the data are encoded by amplitude modulators and coupled into the MVM part of the circuit, where a sequence of WDM demux, amplitude modulators, and WDM mux perform the multiplication part of the computation, and an integrated photodetector combines the beams, returning the final result (fig. 1a). This single vector multiplication can be scaled into a proper MVM directly on-chip (fig. 1b).

We showed, in a previous paper [3], the performance of this ar.96 0 pa7ca(n)5(dlect)2.9(l (dlen)-4(di2((n)5n-2.3(m687 0 344 Tw T*]T

We tested our system with different applications to prove its performance [4]. In the first test, we run an edge detection over the GW face f

[4] Ma, Xiaoxuan, Nicola Peserico, Ahmed Khaled, Zhimo Guo, Behrouz Nouri, Hamed Dalir, Bhavin Shastri, and Volker Sorger. "High-density integrated photonic tensor processing unit with a matrix multiply compiler." (2022).

[5] Peserico, Nicola, Thomas Ferreira de Lima, Paul Prucnal, and Volker J. Sorger. "Emerging devices and packaging strategies for electronic-photonic AI accelerators: opinion." Optical Materials Express 12, no. 4 (2022): 1347-1351.