multiple-access system. The

$\pm 2\pi$

$< 10^{-9}$

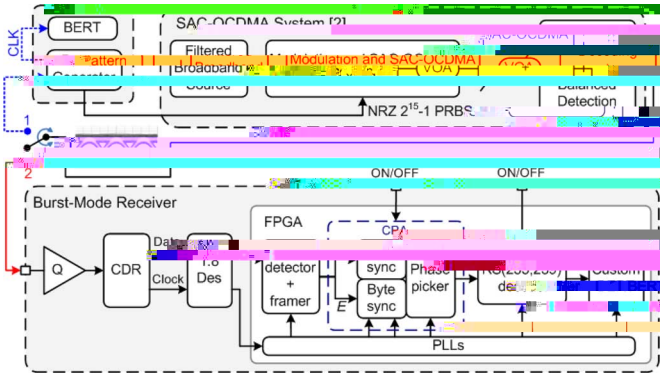

Fig. 1. Block diagram of 7 622 Mb/s SAC-OCDMA experimental setup with the BMRx. PLL: phase-locked loop.

a fourth-order Bessel–Thomson filter whose −3-dB cutoff frequency is 0.7 × bit rate, or 467 MHz. Such a filter reduces intensity noise from the broadband source, while keeping intersymbol interference to a minimum [7]. Bit-error-rate (BER) measurements are then performed with either a global clock, or through our OCDMA BMRx, corresponding to switch position "1" or "2", respectively. To generate alternating packets with adjustable phase, packets from two programmable ports (not shown in Fig. 1) of the pattern generator are concatenated via a power combiner and used to drive the modulator [4]. These packets are formed from preamble bits, delimeter bits, a payload, and comma bits. A phase step and a silence period consisting of an all-zero sequence whose length is equal to the tested number of consecutive identical digits is inserted between packets. The phase steps between packets can be set ±2 ns with 2-ps resolution, corresponding to a ±1.25 unit interval (UI) at 622 Mb/s. Note that 1 UI corresponds to a bit period.

III. SAC-OCDMA Receiver

The SAC-OCDMA receiver we designed is shown in Fig. 1. Our receiver without the CPA apitho2greceip8ia7(e.9626 B)(27(un267)-2na5],n267)-8(b)1reamu24.tn267 cau