Research Article | Vol. 28, No. 8 / 13 April 2020 / Optics Express 11692

Optics EXPRESS

# Lateral bipolar junction transistor on a silicon photonics platform

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**Abstract:** Integration of active electronics into photonic systems is necessary for large-scale photonic integration. While heterogeneous integration leverages high-performance electronics, a monolithic scheme can coexist by aiding the electronic processing, improving overall efficiency. We report a lateral bipolar junction transistor on a commercial silicon photonics foundry process. We achieved a DC current gain of 10 with a Darlington configuration, and using measured S-parameters for a single BJT, the available AC gain was at least 3dB for signal frequencies up to 1.1 GHz. Our single BJT demonstrated a transimpedance of 3.2mS/$\mu$m, which is about 70 times better than existing literature.

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## 1. Introduction

Silicon photonics has become an increasingly popular platform for photonic integrated circuits (PICs), particularly a viable option for low power and cheap photonic interconnects. Progress in integrated silicon photonics technology has resulted in advancement from device-level architectures to large scale integrated systems-on-chip for applications such as communications [1], signal processing [2–4], high-performance computing [5], imaging [6,7], sensing [8], and neuromorphic computing [9]. Optical interconnects based on silicon photonics are becoming ubiquitous in hyper-scale data centers, the centerpiece of the current information infrastructure [1,10]. Silicon photonics is thus establishing itself as a key enabler of the next-generation information and networking technologies.

Current silicon-on-insulator (SOI) photonic integrated technology allows passive optical guiding as well as active optical modulation and photodetection: high-performance Ge-based photodetectors and PN junction based index modulators [11] are already available in commercial silicon photonic foundries' design kits. However, the missing piece in this technology for enabling large-scale photonic systems is the absence of electrical amplification and feedback. Active electronics such as transistors incorporated into systems with high-speed modulators and photodetectors opens up the possibility of engineering highly elaborate photonic systems. These systems also benefit from more efficient optical-electrical (O-E) conversion thereby improving their energy and bandwidth metrics. For instance, Si-based neuromorphic photonic systems that rely on optical-electrical-optical (O-E-O) conversion can enjoy energy-efficient and fast computations when integrated with a transimpedance amplifier (TIA) [9].

There have been two avenues of research in electronic-photonic integration: monolithic and heterogeneous/multi-chip. The major impetus for monolithic integration is the optimization of energy and bandwidth metrics. Most monolithic integration approaches thus far include implementation of photonic devices on various CMOS processes, pioneered by IBM and Luxtera [10,12]. However, historically such integration technologies were disqualified given the intensive customization of processes required to realize photonic systems on a CMOS platform.

#389213 https://doi.org/10.1364/OE.389213
Journal © 2020 Received 29 Jan 2020; revised 19 Mar 2020; accepted 31 Mar 2020; published 6 Apr 2020

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More recently, there have been e orts on novel technology platforms for photonic-electronic integration: namely, CMOS-based *zero-change* platforms [13] and photonic biCMOS platforms [14]. Adapting a new technology platform however entails reinventing the photonics flow by redesigning and recharacterizing individual devices. Alternatively, heterogeneous integration with photonic and electronic chips connected by wire bonds or micro-bumps is another promising path [1,10,15,16]. It allows for optimizing each chip's processing individually, albeit at a small cost of wirebond-induced parasitics. Flip-chip bonding is also emerging as a potential solution to alleviate the parasitics and ensure high bandwidth applications. Even though they require through-oxide-vias (TOVs) [17], which might add complexity to the fabrication process, their overall high-performance makes them the most suitable for our short-term needs.

Given that multi-chip solutions leverage the high performance of mature CMOS electronics, they become indispensable for designing high-performance photonic systems. Nevertheless, they are subject to the limitation of inter-chip pin counts in large scale systems. Monolithic integration on a photonics platform o ers the opportunity of electronic logic and gain, even in a multi-chip integrated system, before packaging-related parasitics kick in. Having on-chip electrical gain can thus supplement the processing done by o -chip electronics. This will inevitably reduce the number of required o -chip connections and their corresponding parasitics. Thus, strides in monolithic integration technology on a photonics platform can mitigate the drawbacks of multi-chip integration.

Prior work targeting electrical gain on a silicon photonic platform includes demonstration of MESFET [18], Germanium-based MOSFET [19], and lateral BJT with gain less than unity [20]. In this work, we demonstrate a lateral BJT with gain on a silicon photonics platform using a standard commercially available foundry process. We achieved a DC current gain of 10, with a Darlington configuration, which is the best performance metric achieved in a commercial silicon photonic platform to the best of our knowledge. Previously, Novack et al. demonstrated a monolithic n-type MESFET on the same platform [18]. With identical fabrication process, their device was subject to the same design rules as ours. To compare their performance against ours: their device demonstrated a transimpedance of 46 $\mu$S/$\mu$m, while our single device fares remarkably well with approximately 70 times higher transimpedance of 3.2 mS/$\mu$m. For a small-signal AC input, under an impedance matched condition, a single BJT can have an AC gain of at least 3dB for frequencies going up to 1.1 GHz.

This paper is organized as follows: section 2 discusses the relevance of a BJT in integrated photonic systems, section 3 details the design of our BJT, and section 4 and 5 present the DC and AC characterization results of our device respectively.

## 2. Monolithically integrated electronic-photonic systems

The promise of photonics beating the bottlenecks of its electrical counterpart, both in terms of speed and energy e ciency, has accelerated advancement in integrated photonic technology. A monolithic electronic-photonic integration scheme o ers advantages including: lower parasitics and reduced laser power requirement over hybrid solutions, thereby enabling low-energy, high throughput density interconnect solutions. A photonic link is comprised of modulators and receivers, where the overall link performance is reliant on the performance of each unit [21]. A gain element, such as a BJT, can be implemented in a modulator driver, and/or in a TIA at the front-end of the receiver to convert small photocurrent from a photodiode to sizable voltage output. However, applications of a BJT extend far beyond photonic links: it can also be valuable for more complex systems like photonic neural networks, where it can enhance the O-E-O conversion, as discussed in [9].

The platform used in this work was primarily optimized for photonic components, like photodetectors and PN junction modulators. Sample characterization results of a microring modulator, MRM, and a Ge-based photodetector on the same chip are shown in Fig. 1. The long

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term goal for photonic engineers would be to incorporate photonic and electronic components into a single system that simultaneously harnesses benefits of both. Currently, the missing piece to realize such a system is an active electronic gain element. With a monolithically integrated BJT, this goal becomes viable. A (non-exhaustive) list of application scenarios of BJTs are presented below:

- Photonic interconnects:

  1. Modulator driver: State-of-the-art index modulators integrated on Si photonic platforms rely on plasma dispersion effect across a PN junction, and typically have $V$ of a few volts [22]. Sample transmitter circuit design, with a microring modulator (MRM), and measured modulation characteristics of the MRM are shown in Fig. 2(a) and 1(c) respectively. Modulator energy cost depends on device parameters (extinction ratio (ER), insertion loss (IL)), and system parameters (data rate). A modulator driver, enabled by a BJT, can reduce the voltage requirement for a certain ER at a desired data rate, improving the overall modulator efficiency.
  2. Receiver front-end: At a photonic receiver, optical data is converted back to electrical domain via a photodiode (PD). The most simple receiver implementation is a resistive receiver, where the circuit consists of a resistor in parallel to a PD before the amplifying stage (PA). With its parasitic capacitance, a resistive receiver suffers from the gain-bandwidth tradeoff, which is avoidable with a TIA [21]. Schematic of a TIA-based receiver is shown in Fig. 2(b). Current Ge photodetectors have responsivity of around 0.7A/W. For optical powers of about -10 dBm, the corresponding photocurrent would be few tens of $\mu$A. A resistive receiver would not suffice to drive a modulator with $V$ of a few volts. TIAs come in handy here as they offer the required voltage swing via photocurrent amplification. Additionally, for high data rate operation, the power budget of a photonic link is primarily dominated by modulator/laser/receiver energy cost over electrical tuning. Improvement in receiver sensitivity via a TIA thus lowers the energy cost of the overall photonic link.

- Computing systems: BJTs can also be used in photonic systems requiring O-E-O conversion, for instance a modulator photonic neuron. Essentially a photonic neuron circuit is a photonic link where a photodiode output drives a modulator via a TIA (refer Fig. 2(c)) .[9] details the significance of using TIAs in such a circuit: transimpedance provided by the TIA was shown to reduce the optical pump power required for the neuron, and achieve 17 times higher gain-bandwidth tradeoff compared to a resistive passive transimpedance. Reduction

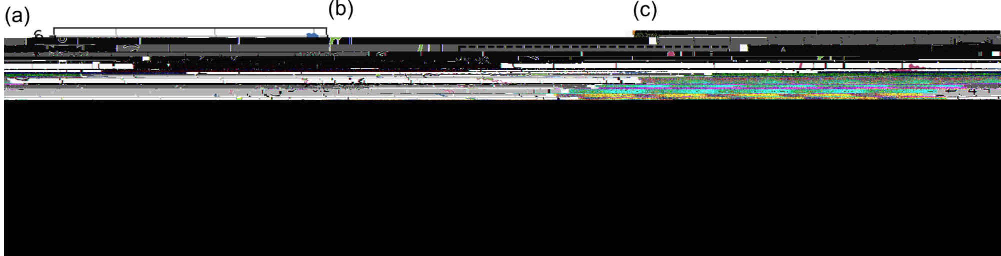


**Fig. 1.** Characterization results of photonic components on the same fabrication run as the BJT. (a) Photodetector dark current at 1550 nm, (b) Zoomed-out plot of (a) showing dark current within reverse bias regime, (c) Eye diagram of a microring modulator modulating 5 Gb/s PRBS pattern with an extinction ratio of 10.4 dB.

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Device performance is inevitably subject to its geometry and doping profile. The foundry reports 10% thickness variation in both silicon rib (220 ± 10 nm) and slab (90 ± 10 nm) layers. They also report width fluctuations of ± 20nm for 500 nm waveguides. Such variation in geometry across a wafer results in fluctuations of BJT resistances and capacitances, which can affect both its current gain characteristics, $\beta$, and bandwidth. Additionally, any variation in doping profile (unreported) directly affects junctions' capacitances, affecting the device bandwidth. Thus some deviation in performance within a wafer can be expected. Another legitimate concern with our design can be potential lattice damage due to successive ion implantation within the transistor, which may occur for high implant energies (above 15 eV). Such lattice damage can manifest as anomalies in electrical characteristics like high leakage currents due to interstitial states [23]. The measured leakage current in our case was in the order of nA, which is more than $10^3$ orders of magnitude below our current operation range. We finally note that this design can be universally applicable to any commercial foundry process offering comparable geometry and doping profiles, as the physics remain the same.

**Table 1. BJT doping density profile and dimensions.**

| Device | Device dimensions [μm] | | | Doping density [cm$^{-3}$] | | |
|---|---|---|---|---|---|---|
| | $L_b$ | $W_b$ | $W$ | Collector (N) | Emitter (N++) | Base (P+) |
| BJT 1 | 3.25 | 0.05 | 0.95 | $10^{17}$ | $10^{20}$ | $10^{19}$ |
| BJT 2 | 4.00 | | | | | |

### 3.1. Simulation using TCAD

Expected device IV curves were simulated using Synopsys' Sentaurus suite. The simulation geometry was defined according to the mask used for manufacturing. Figure 3(a) and (c) show the full device layout and the simulation region respectively. Device fabrication was first modeled with a process simulation using the software's recommended calibrations for silicon. The process included estimates of foundry etching, implantation, and annealing procedures. No posteriori adjustments to fit experimental results were performed. To benchmark the accuracy of this approach, the sheet resistance of the individual doping layers was computed in separate simulations. As reported in Table 2, the simulated values yield tentative agreement with the foundry's reported values for the layers directly involved in the junction (N++, N, and P+).

**Table 2. Comparison of simulated and foundry-reported sheet resistance of individual layers. For the BJT of this work, N++ is used as the emitter and collector contact, N is used as the collector, P++ is used as the base contact, and P+ is used as the base.**

| Layer | Reported sheet resistance ( • ) | Simulated sheet resistance ( • ) |
|---|---|---|
| N++ | 60 | 61 |
| N | 2500 | 2352 |
| P++ | 135 | 80 |
| P+ | 230 | 221 |

Transport simulations were then performed on BJT structures adaptively-remeshed according to doping concentration gradients. Contact electrodes were defined at the upper edges of each contacting region to emulate signals incoming from vias (see Fig. 3(c)). The Poisson-drift-diffusion equations were iteratively solved for various current boundary conditions at the two base electrodes and voltage boundary conditions at the collector electrode. The base current of the simulation is half of the reported $I_b$, since the two simulation base contacts share the same electrode in the physice ina0

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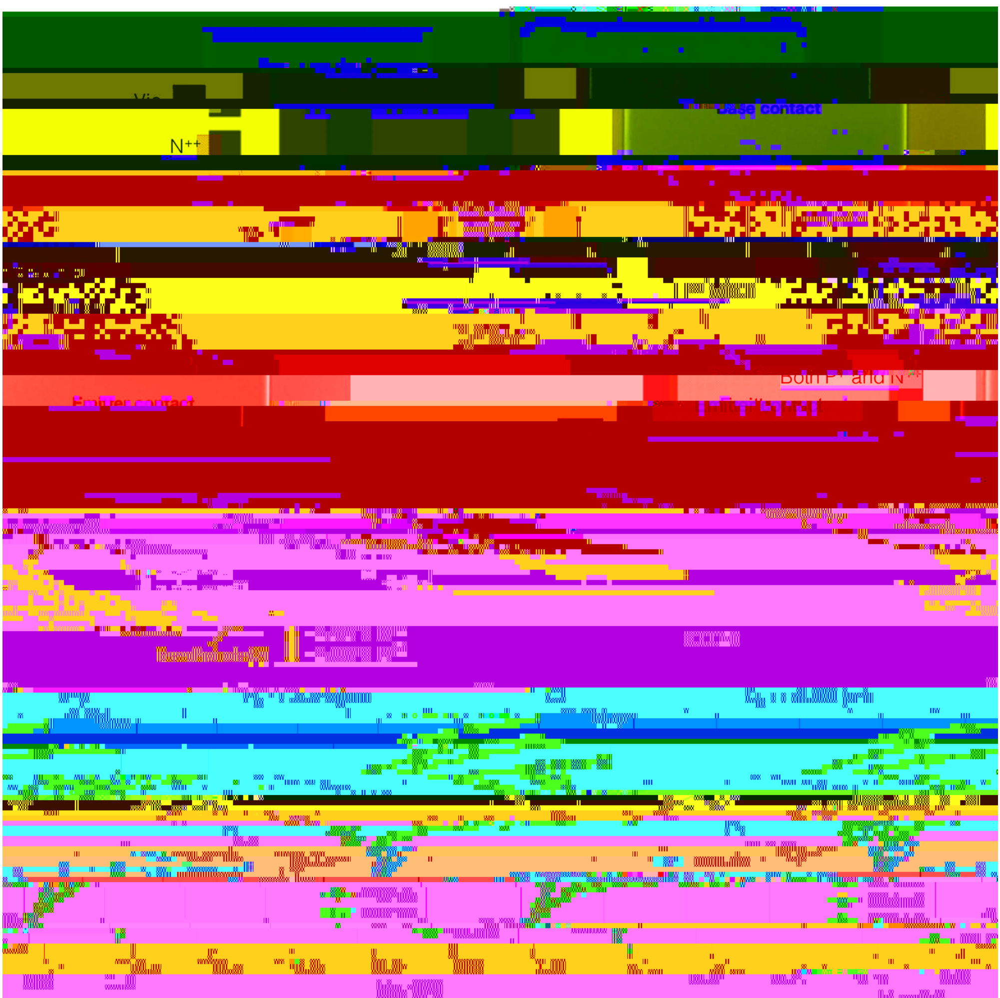


**Fig. 3.** (a) BJT design on Klayout, showing Si and implant layers. The contact pads are connected through metal traces to pads probed for I/O. (b) SEM image of a fabricated BJT on the same chip. False colors overlaid to distinguish di erent doped regions. (Image was taken at PRISM Imaging and Analysis Center, Princeton. (a) and (b) correspond to devices with di erent dimensions.) Device doping profiles obtained from TCAD process simulation: (c) 3D structure of the lateral BJT (denoting the region marked by the dashed rectangle in (b)) showing the activated dopant density profile, (d) device lateral cross-section. TCAD simulation of DC characteristics of the devices with: (e) $L_b$ = 3.25 $\mu$m and (f) $L_b$ = 4.00 $\mu$m.

substrate contact was left floating. These simulation results are presented in Fig. 3.(e) and (f) where expected BJT transconductance characteristics are observed.

## 4. DC characterization

### *4.1. Diode characteristics*

Each BJT has two lateral diodes: the base-collector (BC) and the base-emitter (BE) diodes. Figure 4 shows the experimentally measured *IV* characteristics of each. The measured threshold

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$\beta_R$ (reverse)), saturation current ($I_s$), and Early voltage ($V_A$) were obtained by fitting the data onto the model via Scipy's curve fit function. Each experimental measurement entailed a two-dimensional sweep of $V_{CE}$ and $I_{BE}$ while measuring $I_{CE}$ at each sweep point. Figure 6 shows that the Ebers-Moll model depicts the measured device characteristics remarkably well in both cases. The characteristic parameters of the BJTs are tabulated in Table 3.

Another key metric for characterizing a transistor, especially for TIA applications, is its transimpedance, defined as: $g = \frac{I_{CE}}{V_{BE}} = \frac{I_{CE}}{I_{BE}\, r} = \frac{}{r}$ where $r$ is the BE resistance. With $\beta$ and $r$ obtained from Fig. 4, we can estimate $g$. While a prior work, [18], boasts a transimpedance of 46 $\mu S{\bullet}\mu m$, we achieved 3.22 $mS{\bullet}\mu m$ for our BJT with $L_b$ = 3.25 $\mu$m i.e. about 70 times better (refer Table 3). Additionally, these DC characterization results agree well, albeit not exact, with the TCAD process simulation results discussed in section 3.1. The strong correlation between the process simulation predicted characteristics (see Fig. 3(e), (f)) and the experimental measurements (Fig. 6) suggests that device performance could quite reliably be predicted in advance via our process simulation. Some mismatch between experiment and simulation here

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22.7. A lower measured $\beta$ can be because the bias condition in this measurement di ers from that of a single device owing to the di erence in CE biases: here, $V_{CE,2} = V_{CE,1} + V_{BE,2}$, meaning $V_{CE}$ is always about one $V_{BE}$ higher than a single transistor. This also manifests as an increased *saturation* voltage, i.e. $V_{CE}$ required to reach the active region of operation compared to a single BJT. The dependence of $\beta$ on $V_{CE}$ can be eliminated if there is no dependence of $V_{CE}$ on CE

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## 5. AC characterization

### 5.1. Experimental setup

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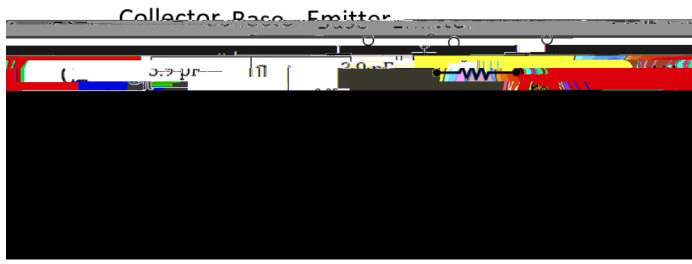

**Fig. 10.** (left) Device cross-section (generated from TCAD simulation) with the equivalent circuit schematic. (right) Parasitics calculated from the measured S-parameters for the following bias condition: $V_{CE}$ = 1 $V$ and $I_{BE}$ = 80 $\mu$A.

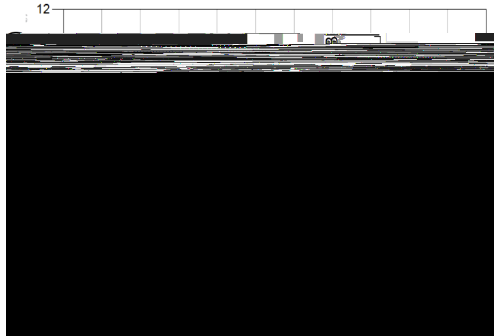

**Fig. 11.** Maximum available gain, $G_{max}$, for a BJT ($L_b$ =3.25$\mu$m) calculated from the measured S-parameters under the following bias: $V_{CE}$ = 1 $V$ and $I_{BE}$ = 80 $\mu$A.

measure of the optimum gain achievable by a device under conjugate matching. Figure 11 shows $G_{max}$ vs signal frequency at a single bias condition ($V_{CE}$ = 1 $V$ and $I_{BE}$ = 80 $\mu$A). It is evident that the BJT can achieve at least 3dB gain within this frequency range.

Typically such impedance matching is done by implementing an LC-based matching network (MN) before and after the device, such that both input and output conjugate matching conditions are satisfied. Using Advanced Design Software(ADS) by Keysight, we designed various input and output LC-based MNs, each optimized for a particular frequency range with a bandwidth

**Fig. 12.** Simulated device AC gain, S21, incorporating matching networks of 200 MHz bandwidth for a BJT ($L_b$ =3.25$\mu$m). The circuit of an LC matching network for 800-1000 MHz is shown as an inset.

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of at least 200 MHz (refer Fig. 12). An MN enhances power transfer to the BJT, inducing gain. Figure 12 shows that aided by MNs, our BJT can provide gain for the entire measured frequency range. The peak gain here ranges from 3 dB to 2.5 dB for frequencies going up to 1.1 GHz. In this simulation, we are interested in having a network with at least 200 MHz bandwidth. The bandwidth-gain tradeo means that our bandwidth constraint reduces the peak gain allowed by a matching network. This is evident in the comparison between the peak gain values in Fig. 11 and 12: the maximum gain in the latter is only 3 dB, while that in the former is significantly higher (above 10 dB).

## 6. Conclusion

We experimentally demonstrated DC gain of 10 with a Darlington configuration of BJTs fabricated on a silicon photonics SOI platform. We also characterized the performance of our BJT under small-signal AC input by measuring the S-parameters, and have reported the device parasitics and the gain metrics. The maximum available gain, with conjugate impedance matching, was calculated to be at least 3dB for measured frequencies up to 1.1 GHz. With impedance matching networks of 200 MHz bandwidth, we can achieve device gain of at least 2.5 dB for the same frequency range. Our active BJT can serve as a fundamental building block in elaborate photonic systems-on-chip.

## Funding

National Science Foundation (EARS-1642962); O ce of Naval Research (N00014-18-1-2297).

## Acknowledgements

The authors would like to thank AMF Pte Ltd., Singapore and CMC, Canada for device fabrication, and the PRISM Imaging and Analysis Center, Princeton for imaging support.

## Disclosures

The authors declare no conflicts of interest.

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