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Primer on silicon neuromorphic photonic processors: architecture and compiler

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Abstract:

Neuromorphic photonic processors are a promising technology for implementing artificial neural networks. This primer provides a comprehensive overview of the architecture and compiler for these devices. The architecture is based on a combination of silicon photonics and neuromorphic computing. The compiler is designed to map high-level neural network descriptions to the underlying hardware. This primer is intended for researchers and engineers interested in the design and implementation of neuromorphic photonic processors.

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3 Photonic information processing

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3.1 Previous decades

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3.3.1 Quantum silicon photonics

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3.3 Contemporary approaches

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Command & Control

5.2.2 Command & control circuit

A Command & Control circuit is used to control the operation of a system. It is a circuit that takes a command and produces a control signal. The command is usually a binary signal, and the control signal is usually a continuous signal. The circuit is designed to be able to handle a wide range of commands and to produce a control signal that is suitable for the system being controlled. The circuit is typically implemented using a microcontroller or a dedicated IC.

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5.2.3 Reconfiguration circuit – interfacing with the real world

Reconfiguration circuit

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Energy efficiency (energy/MAC), throughput per unit area i.e. compute density (MACs/s/mm²), speed (MVM/s), and latency (s), are the key performance indicators (KPIs) for the design of a network. The energy efficiency is defined as the ratio of the total energy consumed by the network to the total number of MACs. The throughput per unit area is defined as the ratio of the total number of MACs to the total area of the network. The speed is defined as the ratio of the total number of MACs to the total latency. The latency is defined as the time taken for a packet to travel from the source to the destination.

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